Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

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**End Semester Examination – Nov/Dec – 2018**

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| **Code : 14EC2032** |  | **Duration :** | **3hrs** |
| **Sub. Name : TESTING FOR EMBEDDED SYSTEM** |  | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Summarize the fault equivalence rules to reduce the number of fault for a combinational circuit. | CO1 | 6 |
| b. | Illustrate the following with examples:   1. 1. Fault dominance 2. Fault collapsing 3. Dominance fault collapsing | CO1 | 8 |
| c. | Elaborate on typical defects in embedded processor chips with examples. | CO1 | 6 |
| (OR) | | | | |
| 2. | a. | List the faults detected and undetected by the input vector 11 for circuit given in figure using deductive fault simulation. | CO1 | 8 |
| b. | Apply Parallel Fault Simulation method and find the faults in the logic circuit given in figure. | CO1 | 8 |
| c. | List the advantages of concurrent fault simulation. | CO1 | 4 |
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| 3. | a. | Generate the test pattern for the combinational circuit given in figure to detect the presence of fault using D-algorithm.  H:\FIG\fig2.bmp | CO2 | 10 |
| b. | Consider the logic circuit shown in the figure Find the Boolean difference with respect to X3. | CO1 | 10 |
| (OR) | | | | |
| 4. | a. | Apply PODEM and find the test pattern generated for the combinational logic circuit for the given figure. | CO2 | 12 |
| b. | Discuss aliasing and its effect on fault coverage. | CO2 | 4 |
| c. | Compare exhaustive and weighted test pattern generation | CO2 | 4 |
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| 5. | a. | Implement the following functions in PLA and consider the cross point between the lines p2 and b4 missing. Apply Deterministic Test generation method to find the test pattern.  F0 = A + B' C' F1 = A C' + A B  F2 = B' C' + A B F3 = B' C + A | CO2 | 14 |
| b. | Discuss the concurrent testable PLA design with a neat block diagram | CO3 | 6 |
| (OR) | | | | |
| 6. | a. | Find the test vector using path sensitization method for the given logic circuit in shown in Figure(6)    Figure(6) | CO2 | 7 |
| b. | Describe the test generation in sequential circuits by time-frame expansion method. | CO3 | 7 |
| c. | Define the following faults that commonly occurs in a memory.  i) Permanent faults ii) intermittent faults iii) pattern-sensitive faults. | CO3 | 6 |
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| 7. | a. | Describe about the test generation algorithms for RAMs. | CO3 | 7 |
| b. | Explain in detail about Scan-in-Scan-out design. | CO3 | 6 |
| c. | Apply LSSD scan path test technique on a SOC and explain with neat diagram. | CO3 | 7 |
| (OR) | | | | |
| 8. | a. | Elaborate the Exhaustive Testing, Pseudorandom testing and Pseudo exhaustive testing methods in test pattern generation for BIST. | CO3 | 14 |
| b. | Explain Ad Hoc testing for design for Testability techniques. | CO3 | 6 |
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|  | | **Compulsory**: |  |  |
| 9. | a. | Justify that “BIST offers various advantages over ATE” and develop a simple Built-In-Self-Test (BIST) for Embedded Systems with a neat block diagram. | CO3 | 15 |
| b. | Discuss the various testing issues in embedded core based systems. | CO3 | 5 |